

ACADEMIC LESSON PLAN FOR WINTER-2025

Dept. of Electronics & Telecommunication, Govt. Polytechnic, Balasore

Name of the Faculty : Jadunath Murmu(Sr. Lect, in E&TC)

DIGITAL ELECTRONICS(ETCPC205)

Theory	: 3 P/W	Progressive Assesment	:30 Mark
Total Periods	: 45P/Sem.	End Sem. Exam	: 70 Mark
Credit	:3	Total Marks	:100
Sem	: 3rd Sem	Start of Class	:14/07/2025

Week	Class Day	Topics
1st	1st	Introduction Logic Gates 1.1 Basic logic gates: OR, AND, and NOT 1.1.1 Truth tables 1.1.2 Logic symbols 1.1.3 Logic voltage levels 1.1.4 Logic circuit design examples
	2nd	1.2 Integrated Circuits 1.3 NOR, NAND, Exclusive OR, and Exclusive NOR gates.
	3rd	1.4 NOR and NAND gates used as inverters. 1.5 Fan-in and fan-out 1.6 Termination of unused inputs
2nd	1st	1.7 AND and OR gates constructed from NAND and NOR gates
	2nd	Boolean Algebra 2.1 Boolean operations (OR, AND, NOT) 2.2 Representation of logic circuits by Boolean expressions.
	3rd	2.3 Laws of Boolean algebra: 2.3.1 Double inversion: $A''=A$ 2.3.2 OR identities: $A+0 = A$, $A+1=1$, $A+A=A$, $A+A'=1$ 2.3.3 AND identities: $A.0=0$, $A.1=A$, $A.A=A$, $A.A'=0$ 2.3.4 Cumulative laws: $A+B=B+A$, $A.B=B.A$ 2.3.5 Associative laws: $(A+B)+C=A+(B+C)$, $(A.B).C=A.(B.C)$ 2.3.6 Distributive laws: $A+(B.C)=(A+B).(A+C)$, $A.(B+C)=A.B+A.C$ 2.3.7 DeMorgan's theorems $(A+B+C+...)'=A'.B'.C'...$, $(A.B.C...)'=A'+B'+C'...$ 2.3.8 Applications to logic circuit simplifications and design
3rd	1st	2.4 Equivalent logic gates 2.5 NAND and NOR implementations of logic circuits.
	2nd	2.6 Standard forms of Boolean expressions 2.6.1 Sum-of-products (SOP) 2.6.2 Product-of-sums (POS) 2.7 Karnaugh mapping
	3rd	2.7 Karnaugh mapping
4th	1st	Combinational Logic Circuits 3.1 Half adder 3.2 Full adder
	2nd	3.3 Half Subtractor 3.4 Full Subtractor
	3rd	3.5 4 bit adder. 3.6 Multiplexer (4:1) 3.7 De- multiplexer (1:4)
5th	1st	3.8 Decoder 3.9 Encoder
	2nd	3.10 Digital comparator (3 Bit)

Week	Class Day	Topics
	3rd	3.11 Seven segment Decoder
6th	1st	Latches & Flip-Flops 4.1. Basic latches 4.1.1 NOR latch 4.1.2 NAND latch 4.1.3 Example uses of latches
	2nd	4.2. Gated latches 4.2.1 Gated S-R latch 4.2.2 Gated D-latch
	3rd	4.3. Flip-flops: 4.3.1 Master-slave and edge-triggered principles
7th	1st	4.3.2 S-R flip-flop
	2nd	4.3.3 D-type flip-flop 4.3.4 J-K flip-flop
	3rd	4.3.5 T-type flip-flop 4.3.6 Flip-flop timing diagrams
8th	1st	Counters 5.1 Circuit diagram and working principle of Binary counters 5.2 up-down counter (circuits, truth tables, and timing diagrams)
	2nd	5.3 Asynchronous counters and ripple counter
	3rd	5.4 Synchronous counters
9th	1st	5.5 Decade counter 5.6 Module-n counter and its combinations
	2nd	5.7. Divide-by-n counters obtained from truncated binary sequences
	3rd	5.8. Synchronous counter design using D-type flip-flops
10th	1st	5.9 Synchronous counter design using J-K flip-flops
	2nd	6.1 Circuit diagram, truth tables, and timing diagrams of Shift Registers
	3rd	6.2 Serial input shift register
11th	1st	6.3 Serial/parallel load shift register
	2nd	6.4 Shift register counters 6.4.1. Ring counter
	3rd	6.4.2. Self-starting ring counter 6.4.3. Johnson counter
12th	1st	Semiconductor Memories 7.1 Define the terms ROM, RAM, PROM, EPROM.
	2nd	7.2 Draw a typical memory cell
	3rd	7.3 Design a small diode matrix ROM to serve as a code converter.
13th	1st	7.4 Design and draw the logic diagram of a specified size memory system
	2nd	7.5 Operating principle of dynamic memory
	3rd	7.6 Advantages and disadvantages of dynamic memory vs. static memory
14th	1st	7.7 Difference between dynamic memory vs. static memory
	2nd	Sequential Circuit Design 8.1 Combinational vs. Sequential circuits
	3rd	8.2 Adder, Subtractor, decoder, multiplexer, de-multiplexer, and comparator
15th	1st	8.2 Adder, Subtractor, decoder, multiplexer, de-multiplexer, and comparator
	2nd	8.2 Adder, Subtractor, decoder, multiplexer, de-multiplexer, and comparator
	3rd	8.3. Finite state machines- Concept only


 Signature of Sr.Lect./Lect.


 Signature of HOD