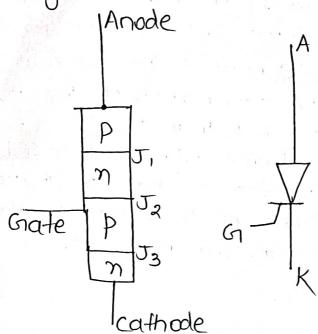
LECTURE NOTES ON POWER ELECTRONICS & PLC (TH-5) DIPLOMA COURSES 5™ SEMESTER ELECTRICAL ENGINNERING

PREPARED BY- ER. RADHA RANI PANDA (LECT. ELECTRICAL)

DEPT. OF ELECTRICAL ENGINEERING
GOVT. POLYTECHNIC BALASORE

Ol:	Cowle
Objectives of the Lecture	Construction, Operation, V-1 characteristics & Application of Power
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	Thyristor is a family of power semiconductor switching devices. The thyristor has four or more layer and 3 or more 'Junctions. The name of the thyristor is derived by the combination of the capital letters from THYRATRON and transistor i.e. Thyristor is a solid state device like a transistor and has characteristics similar to that of thyratron tube. Members of thyristor family are > SCR-Silicon controlled Rectifier. > Diac > Triac > GTO (Gate Turned OFF) > Sus-(silicon Unilateral switch) > SBS > LASIR - Light activated SCR principle of Operation of SCR;
	Thyrastore is a foure layers, three Junction,
1	3 terminals, Anode, cathodes jare in consists of four alterenate p-type & n-type semiconductors
63	An SCR is so called because silicon is used forc its construction and its operation as a rectifierc can be contralled.

-> Thyrristore is a unidirectional device.
-> normally gate terminal is provided at the p-layer near the cathode.



the device.

* Silicon provides good thate terminal theremal conductivity high voltage and current papability. * Cathode is must heavily doped that and anode are next heavily doped, lowest doping is switch central in layer.

The when Anode is made positive which cathode, I so Is are forcinated biased but Iz is reverse biased. Thus sunction Iz due to present of depletion layer doesn't allow any current to flow through the device. Only leakage current of small magnitude flows due to drift of mobile charges which is insufficient to make the device conduct. This is called

Foreward blocking state ore OFF State Fore

7 Anode & Cathode arre connected to main Es X Source through the load. The gate and cathode are fed from a Source Es which provides positive gate to Current. Generally thyrastore has three basic modes of opercution > Reverse blocking mode > forward blocking made > forcuard conduction made. Reverse blocking mode: When cathode is made positive but anode with switch 's' open, thyrastorc is rreverse biased Junction J, J3 are rreverse biased and Jz is foreward biased. Thereeforce a small leakage current Flows (MA). The reverse blocking mode is called the OFF state and shown by op 7 If the reverse voltage is increased then at a crátical level, called reverse breakdown voltage (VBR), an avalanche occurs at J, 8 Ja & rreverge contrent increases trapidly. 7 If the current isn't limited to a safe value power dissipation will increase to a dangerroug level that may destroy the device pais the reverge avalanche region.

-> when the Cathode is made positive write anode, Ja is fortwared biased whereas I, and I is reverge biased only a small leakage current flows where which is insufficient to make the device conduct on off state. 7 The width of depletion layer at Ja decreases with increase in anode to cathode voltage and at a stage depletion loyer of J2 a varinishes. 7 The reverge biased Junction Ja breakdown due to large valtage gradient across it & the phenomenon called as Avalanche brieakdown. 7 P Now J, J2 & J3 are forcward biased, so, large amount of current flows through the device. 7 The device starts conducting and called as conducting State or on State. Static Anode - cathode charcacteristics of SCR _ forward conduction TOA latching current Holding current Ig3, Ig2 I31 VBR Forward reakage current Reverse Forcwared leakage blocking currient Mode Reverse Blocking Mode LIa

The reverse voltage applied across the device is below VBR, the device will behave as a high impedance device in the reverse region.

* Forcward Blocking region:

When anode is positive writt cathode, with gate open, thyrastori is said to be forward biased.

Thereforce, J., J. arce forcward biased while Ja is reverge biased and a small leakage current called forcward leakage current flows through the device.

As forward leakage current is small, SCR offers a high impedance.

> Thyraistor can be traeated as an open Switch in Fortward blocking mode.

Forcward Conduction Region:

When anode to cathode forcovaried voltage is increased with gate CK+ open, reverge biased Junction Jz will have an avalanche breakdown at a voltage called forcovaried Breakovere voltage VBO.

Tybo is corruesponding to 'M', when the device latches on to conduction State.

The device latches on to its on state, the voltage across the device drops from several volt to 1-2 volts, depending on rating of scr and suddenly a large amount of current stards flowing.

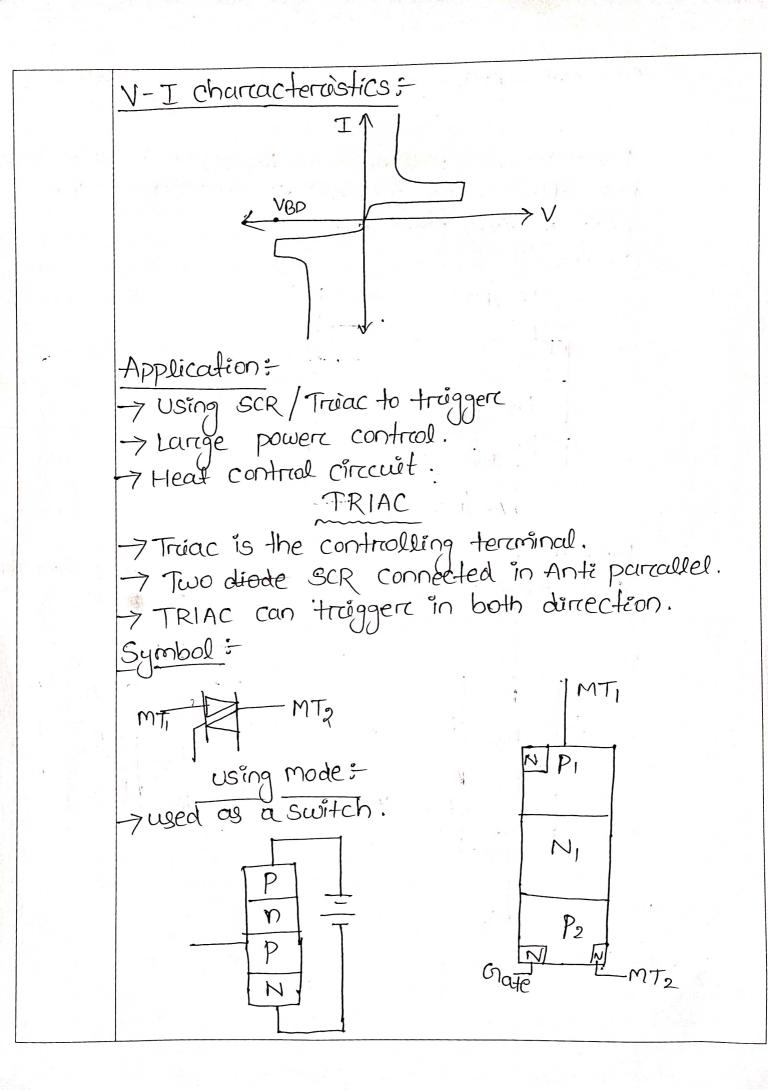
This characteristic is called forcward conduction State and Thyrastore tereated as a open Switch. Twhen gate signal is applied, thyrastore turns on before VBO reached. The forcward Voltage at which the device turns on depends upon the magnitude of gate current.

The magnitude of gate signal increases, the voltage at which the thyrastore turns on decreases.

The voltage at which the thyrastore turns on decreases.

The voltage of the current of the voltage of turns on the voltage of the voltage of turns on the voltage of the voltage of the thyrastore turns on the voltage of the voltage

Objectives of the Lecture	
Learning Outcomes	Construction, Opercation, V-1 characteristics & application of DIAC, TRIAC.
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	Diac is the bidirentional device 1t is the Diode force alternating current combination of two diede in Anti parallel. Construction: A,
	Norcking: A_2 / MT_2 Working: A1 is more + Ve + Han A2 A2 is more + Ve + Han A1 $A_1 / M_2 / M_3 / M_4 / M_5 / M_6 / M_7 / M_8 / M_$



Application :

> Lamp control.

> chopper

-> As phage control.

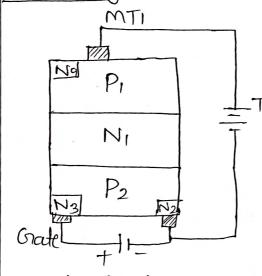
Defination:

TRIAC is a bothree ele-three terminal electronic component that conducts current in either direction when triggerred

7A Trojac can work both direction.

7 It is a bidirectional device.

Wordking >



2	
$MT_2(t)$ $CD(-)$	$MT_2(+), G(+)$
MT ₂ (-)	MT2(-) (n@(+)

Quadreab/-1

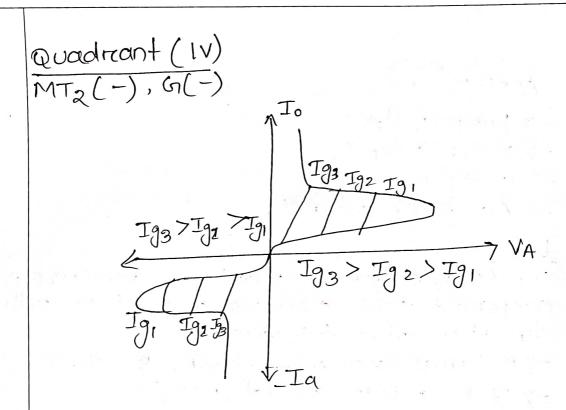
is the most sensitive (i.e least gate current) required to turned on the device.

Quadrant-11

MTz, G- Modercate.

Quadrant - 111

MT2(-), G(-) is the least sensitive (most gate current required to turned on the device)



Objectives of	T 1 20 000
the Lecture	Two transistors analogy of SCR.
Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
	The operation of SCR can also be explained by considering it in terms of two transistors, known as two transistors analogy of thyrastors. 7 This madel is obtained by spilling the two middle layers of SCR into two Separate parts & SCR can be considered as an open mpn & pnp transistor. A VIA P Ty Ty Ty Ty Ty Ty Ty Ty Ty
	Forc Transistore T2 IE2 = IK
	$I_{B_2} = I_{B_2}$
	From the above Figure 1t is observed that the collector current of T_1 becomes base current of T_2 8 viceverge · also $T_1 = T_1 + T_2 = T_1 + T_2 = T_1 + T_2 = T_$

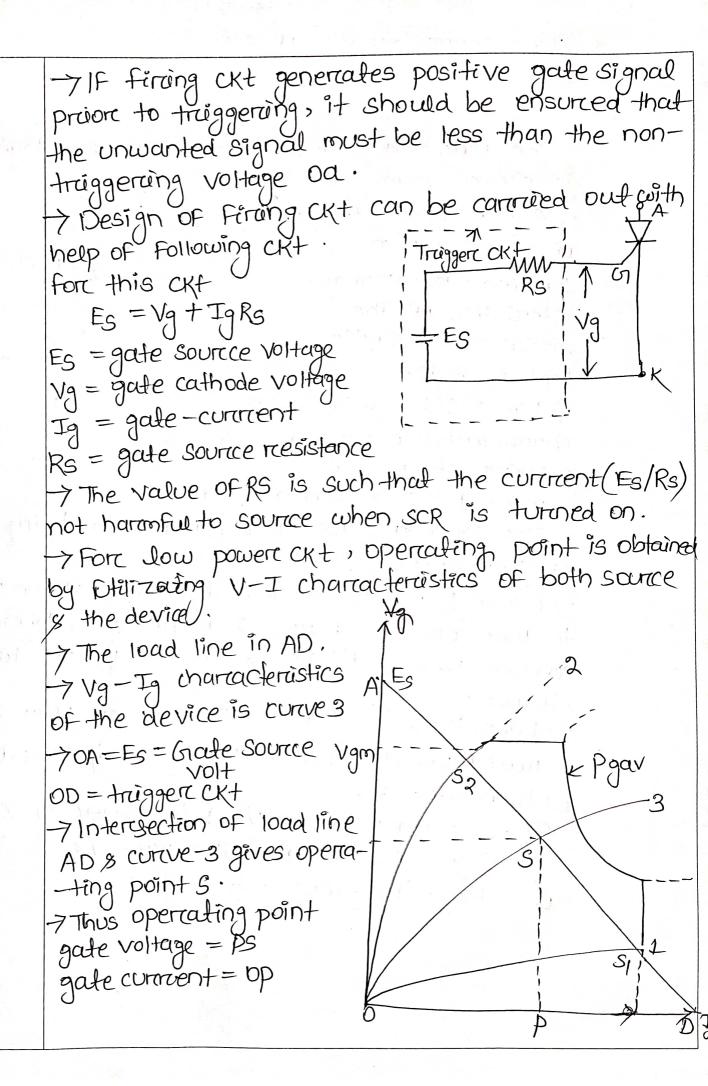
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In the OFF State of a transistor,
     Ic = d IE + ICBO
d = Common bresse currient quin
ICBO = Common base cui learage current of collectors
       base Junction.
FOR Ti,
     Ic, = d, IE, +IcBOI
    => Ic, = d, Ia + IcBo, ---- (1)
Forc Iz,
IC_2 = d_2 I_{E_2} + I_{CBO_2}
      > Ic2 = d2 Ix + ICBO2-
The Sum of two collectors current is equal to the
exterenal ckt current Ia entering at anode
terminal. Ia = Ic, + Ic2
      => Ta= d, Ia+ IcBo, + d2 Ix + IcBo2
      => Ia = d, Ia +d2 (Ia+Ig) +IcBo, +IcBo2
      => Ia(1-d1-d2)=d2 Ig+ IcBO,+ IcBO2
      => Ia = d2 Ig + IcBo1 + IcBO2
                     1-(d1+d2)
7 Forc a Silicon transistor
                               dr
d is very low, at low voltage
value of IE · d build up
                              0.75
rapidly as the emitter
                              0.5+
current increases.
                              0.25
                                 \circ
```

> With Ig = 0, if emitter current of two transistor cure increased so, that of the 2 = 1, then as per eq? — 3, Ia would be tend to become infinity.

> As the anode current attains high value, the device suddenly latches into conduction (ON) state from off state. This characteristics of

device is known as Regenercative Action.

Objectives of	Grate characteristics of SCR.
the Lecture Learning	· · · · · · · · · · · · · · · · · · ·
Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
	The Foreward gate characteristics of a thyroistor
	is shown below. Vgn c-12
Actual lecture in	> A gate cathode CKt vgnf
details with	of scr is a p-n
fig.	Junction, gate chara-
1.1	LCtercistics of the //
	device are similar to
1,6	that of diode.
	characteristics has a g
	characteristics has a 19
TA TH	a speed between two X Ign Ign
(1"1 1	curives 1 8 2 as shown in Fg.
in the continue	-> The speed onis due to difference in doping level
B NITTO Y	of pan layers.
	-> curive 1 repræsents lowest voltage value applied
	to turn-on SCR. kureve-2 represents highest
	voltage value that can be safely applied to gate
	ا مُنْ مِنْ مِنْ اللَّهِ مِنْ مُنْ اللَّهِ مِنْ مُنْ اللَّهِ مِنْ مُنْ اللَّهِ مِنْ مُنْ اللَّهِ مُنْ اللَّهِ
	-> Each thyrristore has maxin limits as vgm & Igm
1.1.	& realed powere dissipation pgav specified force
- 1.	each other SCR.
	each other SCR. Oy, OX = Minimum gate Vs I to trigger an SCR.
	Yan, Lam = Max, bellions, or Jac V
	oa = Non - traggerang gate voltage.



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The operating point 's' may change from Sitoso & it must lie within curive 1 & curive 2.
7 The gradient of load line AD will give the
raguiral rate of source rasistance Rs.
7 Frequency of Firting forc trugger pulse can be obtained by taking pulse of
  (i) Amplitude (Pgm)
  (i) pulse Width (T)
 (iii) perciodicity (Ti)
 Pgm. Pgm T > Pgav F= = Frequency of
Ti Fircing (Hz)

=> Pgm · T. F > Pgav T= Pulse width (sec)
    => Pgav < pgm
In the limiting case, Pgm = \frac{PgaV}{FT}, f = \frac{PgaV}{T \cdot Pgm}
7 Duty cycle is defined as the
 realio of pulse on perciod to perciodic time of
         S = \frac{T}{T_1} = FT
  Pgav & Pgm
 => Pgav = pgm
```

e*	
Objectives of the Lecture	Switching characteristics of SCR during & turn on.
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
	Turch - ON
Actual lecture in details with fig.	7 A fortward biased thyrustore is turned on by applying a positive gate terminal bisignal bet gate & cathode. 7 The time during which the SCR changes From Fortward blocking state to fortward conduction state is called as turn on time.
	Turn-on time is divided into three intervals.
	ii) Delay time (td) iii) Rise time (tr.) node vatage Vo 1A o-9 va o-1 va on state voltage drop voltage current iTa=load current
a, is per.	Ia Recombination
OV Cu	orcward that the the the tree the tree to the top top to the top top to the top
,	TURN ON & TURN OFF

i) Delay Time: It is defined as the time during which anode voltage falls from Va to 0.9 Va where va is the initial value of anode voltage. 7 It may be defined as the time during which anode currient raises from forcward leakage current to 0.1 Ia. Ia = final value of anode currient. 7 Delay time = time perciod between 0.9 Ig to 0.1 Ia. > Durang delay time, anode rurrient flows in a narrrow region near the gate where current density is highest > Delay time can be decreased by applying high gate current & morre forcward anode to cathode voltage. Ig 1, d Ig 1, cathode conduction arrea 1 => ta V ii) Rise time :-The Rise time is the time taken by the anode current to reise from 0.1 Ia to 0.9 Ia.

current to reise from 0.1 In to 0.9 In.

To During this period, anode current flows almost entire cross-section of SCR.

Tre, inversely propertional to the magnitude of gate current and its build up reale, which depends on the load CKt parameters.

The a RL CKt, if L is high

d Ig +, tre 1

It is the time taken by the anode current to raise from 0.9 In to In.

During this time conduction sprands over the entire-crosssection of SCR.

It depends on the structure of the device '

Ton = to + trc + tp.

Turnon time depends on following parameters.

i) Grafe current

Ig1, of Ig1, to V, ton V

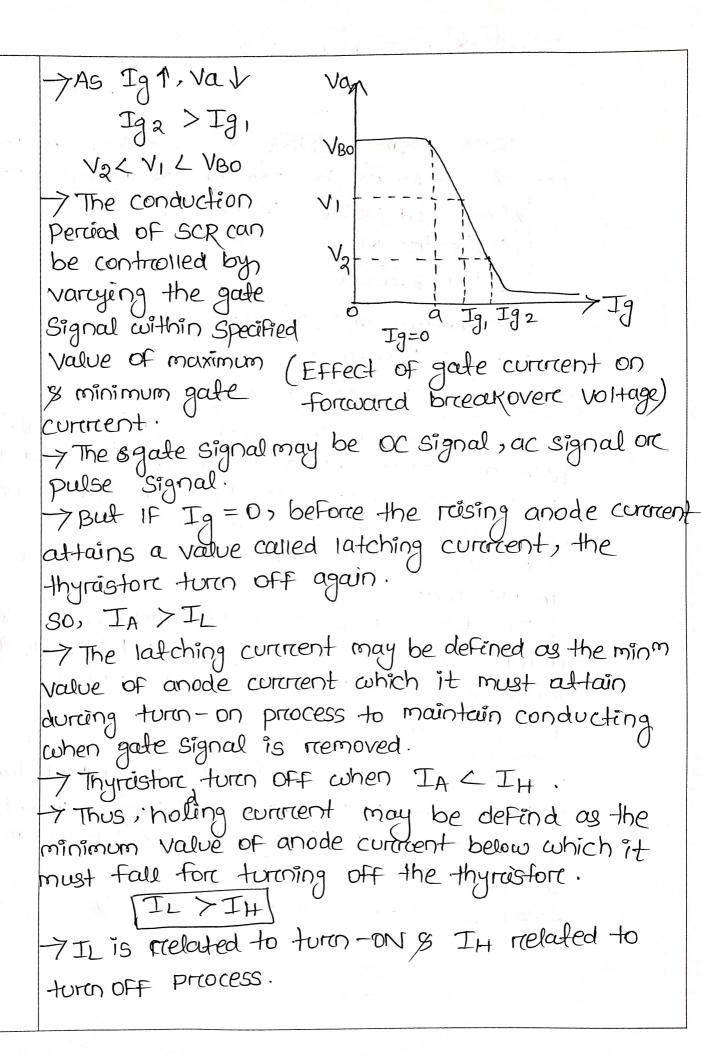
ii) Load CKt parametere.

Objectives of the Lecture	Switching characteristics of SCR during turn an OFF.
Learning Outcomes	0.
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	Turn OFF (tq): The process of turning off a thyrastore is called as commutatation. The dynamic process of SCR from conduction state to forward blocking state is called turn -OFF process. The opening of a thyrastore is on, gate loses control, SCR
	turned off by reeducing anode correct below holding current is by applying a reverge voltage of turn off time, to of a thyristore is defined as the time between the instant Ia = 0 and the instance SCR reguins forward blocking capability. I turn off time divided into two interevals. i) Reverse vecovery time (t) ii) Gate recovery time (t) to = true + tgre
Hayana Janaa	The time taken to remove the charge carriers from the outer tayers of SCR is called reverse recovery time (trin) the best to \$1 \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$

anode voltage is developed & reverge recovery current continues to decrease. -7 At t3, J1, J3 are able to block reverge voltage. (ii) Grate Recovery time : The time required to develop potential barciciere in Iz is called Recombination time orc gate recovery time (tgre) beto t3 8 tu. 7 At t3, 1 J2 Still contains charged carcriters zoe trapped charges. so SCR is n't able to block forward voltage. 7 The trapped charges around Jz Te innere two layers are removed by Recombination (automotic neutralisation of charges among themselves is called Recombination). 7 During turn off time all the excess charge carriers are completely removed. 7 tg depends on magnitude of anode current, di & Junction temp i) ckt turn-off time (tc) = -> If is the time for which the comutation circuit appoires a reverse voltage across the device after the anode current is zerro. tc > tq. -> The commutation cut must apply a reverse voltage across the device during turn off fore successfull commutation. 7 (5m) tq

SM = Saffy margin.

Objectives of	
the Lecture Learning	Turn ON methods of SCR.
Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	With anode positive wire-t cathode, a thyrastore can be turned on by one of the following methods i) Forcwared voltage traggering ii) Grate traggering. iii) dv traggering iv) Temercature traggering
Y . 1 . 1 . 1	V) Light treiggereing.
(1 3 1 1 4 1	i) Forcward voltage traggering &
	When anode to cathode voltage is increased with gate circuit open, the reverge biased Junction Is will have avalanches breakdown at a voltage
rana sal	The forward voltage - drop across the SCR during the ON State is 1 to 101.5 V and increases slightly with load current.
1 1 1 7 1 1	ii) Gate Traggerang :
	Tsimple, reliable & efficient method of triggering. The applying a positive signal to gate w.r. t cathode the device can be traggered much before the specified break over voltage. The specified break over voltage. The specified break over voltage.



(iii) dy Truggerung:

With forcward voltage across the anode 8 cathode of SCR, J, 8 J3 arce forcward biased but inner Junction J2 is referreverse biased.

7 The reverge biased Junction Jz behaves as a capacitore due to charge existing across the Junction.

7 IF forward voltage is suddenly applied, a charging current through Junction capacitance C; may turn on the SCR.

71F fortward voltage Va appears across J_2 charging contrent $\dot{\epsilon}_C = \frac{dQ}{dt} = \frac{d}{dt} (c_3 \cdot Va)$

 $\dot{z}_c = C\dot{z}\frac{dVq}{dt}$

= C; dva + Va dci dt dt (dci=0

750, if dva is high, ic is high.

and turns on the SCR even though Ig=0.

(iv) Tempercature Traggering:

The width of the depletion layer of SCR decreases on increasing the Junction temperature 7 when temperature is increased near the reverse biased Junction more number of es holes pairs are produced.

JAt a point, this initiates turn on process of the device.

For light Troiggereing:

For light troiggered SCR a

recess/inche is made in the
inner p-layer.

Thus, the number of charge

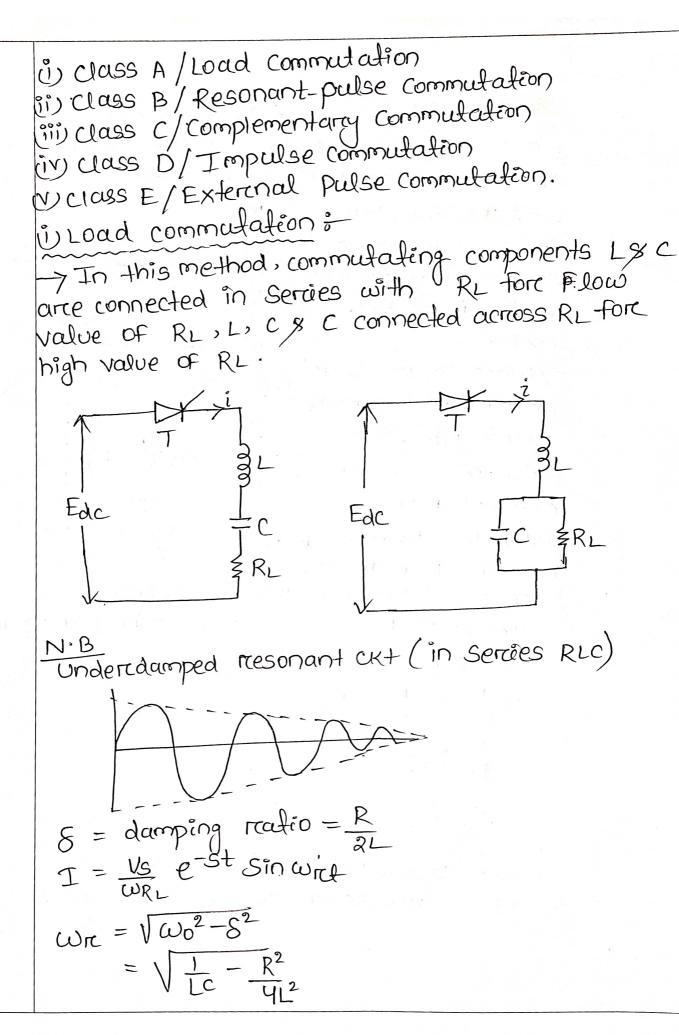
Cartriers are increased which lead to instantaneous

Flow of current and the device is troiggered.

Tused in LASCR (Light Activated SCR).

Objectives of the Lecture	Turch OFF methods OF SCR (Line Commutation & forced Commutation) Load Commutation.
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
	Turch of Methods of SCR
Actual lecture in details with fig.	The turning off process of thyroistore is called as commutation. Thyroistore Commutation watechniques use resonant LC ore undercidamped RLC circuits, to force the current/voltage of a thyroistore to zero to turn off the device. There are two methods of commutation.
	i) Natural commutation i) Forced commutation
	i) Natural commutation: Tris method uses alterenating, reversing nature of A·C Voltages to effect the current transfere.
	DVs=Vm Vo ZR Sinwt Vo Sinwt 27
	JT 1-4m /2JT 3J1

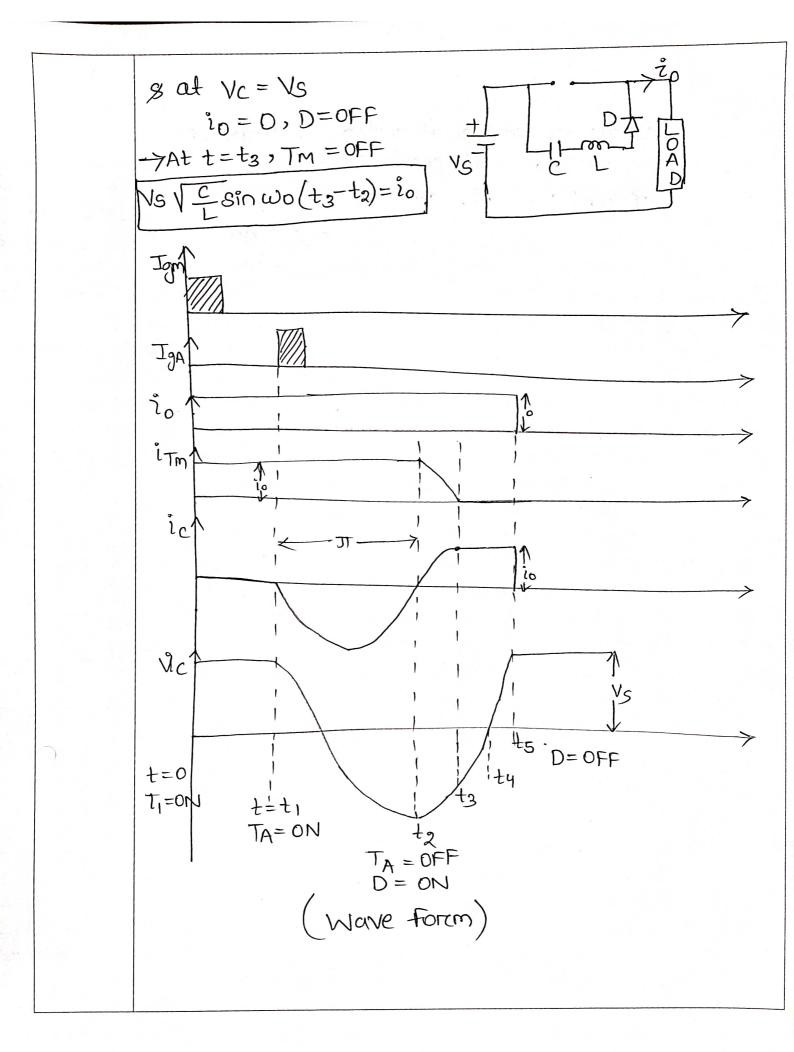
> During positive half cycle of SCR is traggered and conducts currents. When ac voltage = 0 at Wt = JT, Also Ia = 0, Forc R load. TAFter anode current has reduced to Zerro, ac source applies a negative voltage across the SCR forc Sometime Forc turning off the SCR naturally 7 This method is applied to phase - controlled converders, ac voltage controller l'ine commutated inverders. 7 Thyrastoris reverge biased for a perciod IT. Jr = cotc >tc=J/w /tc>tal 7 This method is also known as Line commutation orc class of commutation. ij forcced commutation: 7 It is used us fore dc Supply. In dc ckt forc Switching off the thyroistore, the Forcward current should be forced to Zerco by means of some exterenal CKt. > This process is called forced cond commutation and exterenal ckt required fore it is called commutation CKt. 7 The commutation cxt develops a reverse voltage across the SCR which brings the forcward current to zerco, thus turning off the device. -> Forced commutation is divided into following types depending on the arrangement of commutation components.



7 The Load Resistance RL & Commutating components L& C, So, selected that their combination forces an underedumped resonant ckt. 7 In this CKt, SCR conducts & carries Edc the charging current in the first half. eycle. Twhen the capacitors Isa voltage Edc, the J/W/K Edc value of charging vs current decays to a value less than holding current for device. > This switches off the thyrastore. -> In serves RLC CKt , forc underedamped condition. wre >0 > LC - RL2 >0 > Lc > RL2 =>RL JYL & SCR opercated For IT/wr Sec. 7 It is also known as Self commutation

Objectives of the Lecture	Resonant Pulse Commutation.
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	In this method main SCR commutates due to an equal amount of capacitors discharges current in opposite direction to the main SCR current. VS T T T T VO AD
did diena	7 Tm = Main thyrristore which carcries Load current. 7 TA = Auxilliary thyrristore which helps to commutate Tm.
11.1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1	Thisally Tm & TA are OFF and the capacitore is charged to Vs with left plate positive. Vc = Vs (+11) At t = 0, Tm is truggerced and constant load current io is established in 1 the load CKt.
	So, iTm = io, Vc = Vs, ic = 0 To. Commutate the main SCR (Tm), Ta is traggerred. at t = t1, Ta = ON. Thence, capacitors finds a closed path 3 discharges through (ct - Ta - L - 4c) 8 then charges with reight plate tve i.e Vc = Vs (11t)

THENCE, capacitor Finds a closed path & discharge through $(C^{\dagger} - TA - L - C^{-})$ and then charges with reight plate + Ve. i.e Vc = Vs (11+) The magnitude of the discharge current Ee ic = -VsV - sin wot Tic = -Ipsin wot -ve sign indicates that current flows opposite to the reference the direction of ¿c. Capacifore Voltage Vc = 1 (icdt Vc = Vs cas wot ->t=t2, Vc=-Vs i.e (aftercJT readians fromt) TA is rreverse biased & commutated. -> AFter TA DFF, capacitor finds a closed ckt. L. D8 Tm & capacitore discharge in opposite dirento itm. so, net forcward current $\hat{i}_{T_1} = \hat{i}_0 - \hat{i}_C$ AS 2ct ît, V > when ic attains value of 20,2 Tm is reduced to zerro value & Tm is turned off at ta. -> AFter Tm = OFF, Io flows from Vs to load through C, L & D. & capacitore charges with left plate positive- te vc = Vs (+11)



Capacitare voltage at which Tm turns off => Vcq = Vs $cas wo (t_3-t_2)$ circuit turn off time = $tc = ty-t_3$ = $C \cdot \frac{Vab}{lo}$

Objectives of the Lecture	Protection of SCR, over voltage protection, over current
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	Marker Pen, Duster, White board, Projector All powers devices have specific realings & for recliable satisfactory operation its realings must not be exceeded. If a device experciences overs voltage or high current, It may be destroyed so, the device must be protected against abnormal condition. di preotection: at when SCR is forward biased by a gate value, when SCR is forward biased by a gate value, the current spreads across the whole area of Junction. It has realing > spread velocity of charge carrivers, local notspot will be formed & the device may be damaged. To limit the dia small inductors is connected in Sercies with the SCR. This inductors called as di inductors/current so: Snubbers. dv protection: dv protection: dv protection: dv protection: dv protection of the SCR ckt. To limit the dv, snubbers ckt is connected in dr parallel with the device.

Objectives of the Lecture	Firting Circuits, General layout diagram of firting circuit.
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with	An SCR can be switched from OFF State to ON State by Severcal ways ite forcward voltage traggering Light traggering, dydt traggering, Temp traggering, gate traggering.
fig.	The ckt which produces necessary gate signal to turn on the SCR at desirced instant of time is
	called firting circuit / Iraiggerang CRt.
	Firting of Thy reistore;
\$ 5 P 169	The basic requirement for successful firting of a thyristor are their the current supplied to
	the gate should i) to be adequate amplitude & short ruse time.
1 1 2 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	ij be of adequate duration ij occurre at a time when main ckt conditions
y to jet	are favourable of conduction.
0, 51,	Grate Current Amplitude:
	Ty Igmin is the minimum gate current required to fit all thyrristore of same type at a standard temperature.
	current is satisfactory so long as main ckt don't
	have special requirements. The firting current is high then turn on time treduces The specification of gate current amplitude
	is incomplete without rase time.
4	

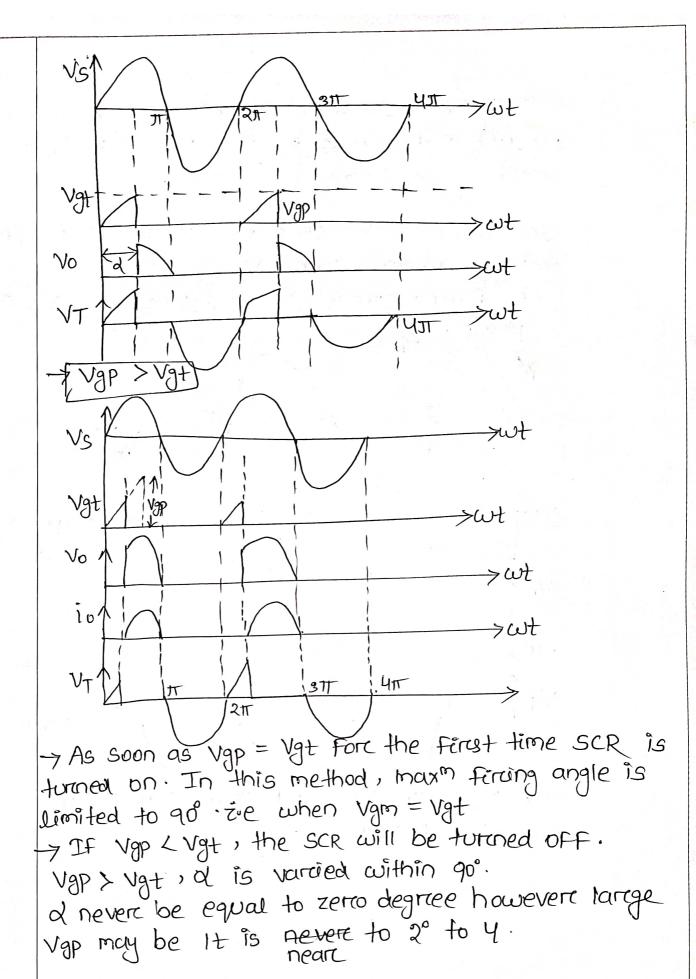
"> Effectiveness of pulse increases by the raise time is reduced. Grate pulse duration: 7 A thyraistore may be traggered successfully by a gate pulse of a duration approximally equal to furn-on time of the device. > But longer pulse duration is desircable for the following reasons. DA relatively long perciod may be required for the anode current to raise to the latching current level. in Oscillation reflections or other distrubances may conspire to turn off the SCR shortly after it is first traggerred. 7 In general pulse duration of less than lows requires in the design of anode cut, while a duration of 30-days is sufficient to avoid problem as long as anode cut cond are favourable to conduction. Grate Traggering Ckt: AC Pulse Pulse generator amplifier 1/p Dc powerc Supply Tree Min V.d -Driver ckt ----*control CK+--power. (General Layout of firing ckt

Firting ckt has two functions:

i) IF power ckt has to morre than one SCR, the
firting ckt should produce pulse for each SCR at
desirted instant for proper operation.

Objectives of the Lecture	R Firting circuits.
Learning Outcomes	0
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	R ₂ = Variable resistance which charges firing of gate value is gives the variable timing angle: R = Stabilizing P = used to limit the Vs gate voltage with in permissible value. R ₁ = is added to limit the gate current within permissible value. Firting In case R ₂ = 0 gate current Flows from source, through load R ₁ × gate to cathode. The current showlit enterted max m permissible gate current Igm. Load resistance = Max voltage = Vm Vm R ₁ = Igm orc R ₁ > Vm Tgm R ishould have such value that max current across it doesn't exceed max gate voltage Vgm. Mox current possing throug R, = Vm R ₁ +R

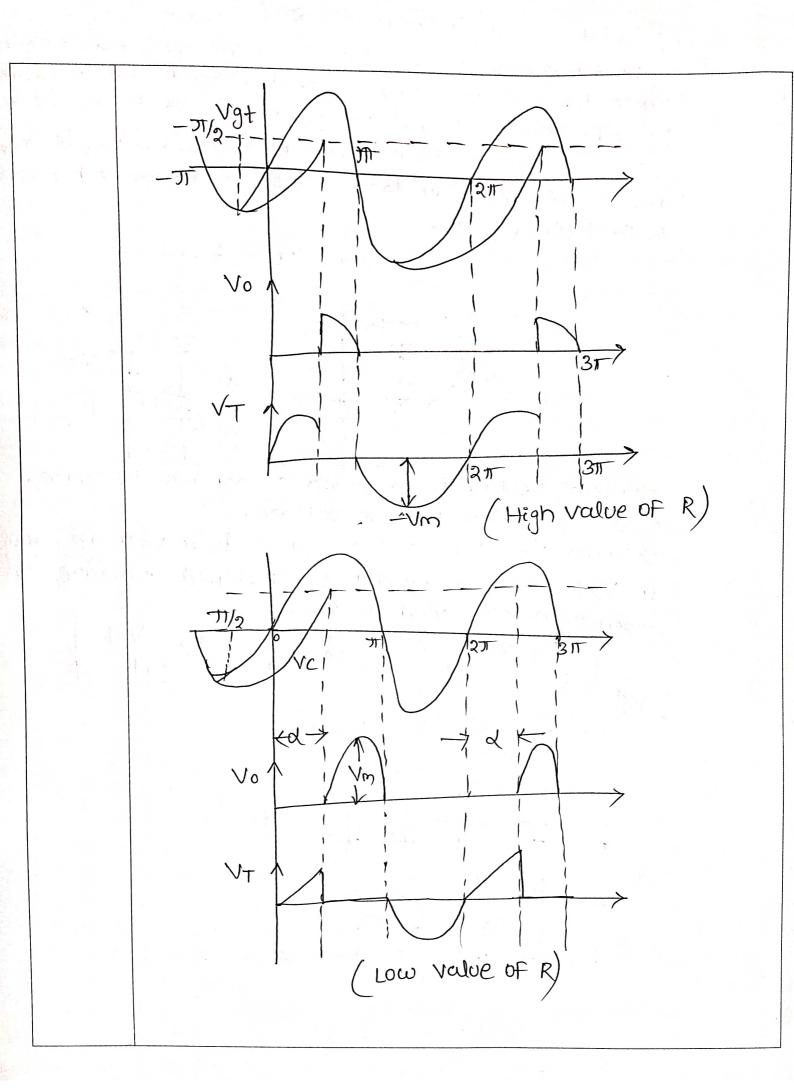
TF R2 is large, current i is small, as to mesult v.d across R, t.e Vg = i.R is also Small · Vgp L Vgt SCR will n't turn on & Vo = 0, io = 0 & supply voltage apperarcs across VT. 7 As firting circuit is resistive yg & Vs arce in phase. < Vmsinat Vs1\ Vgp L Vgt vgt Vo · lo VT →wt 71f Ra is so adjusted that | Vgp = Vgt then D=90°

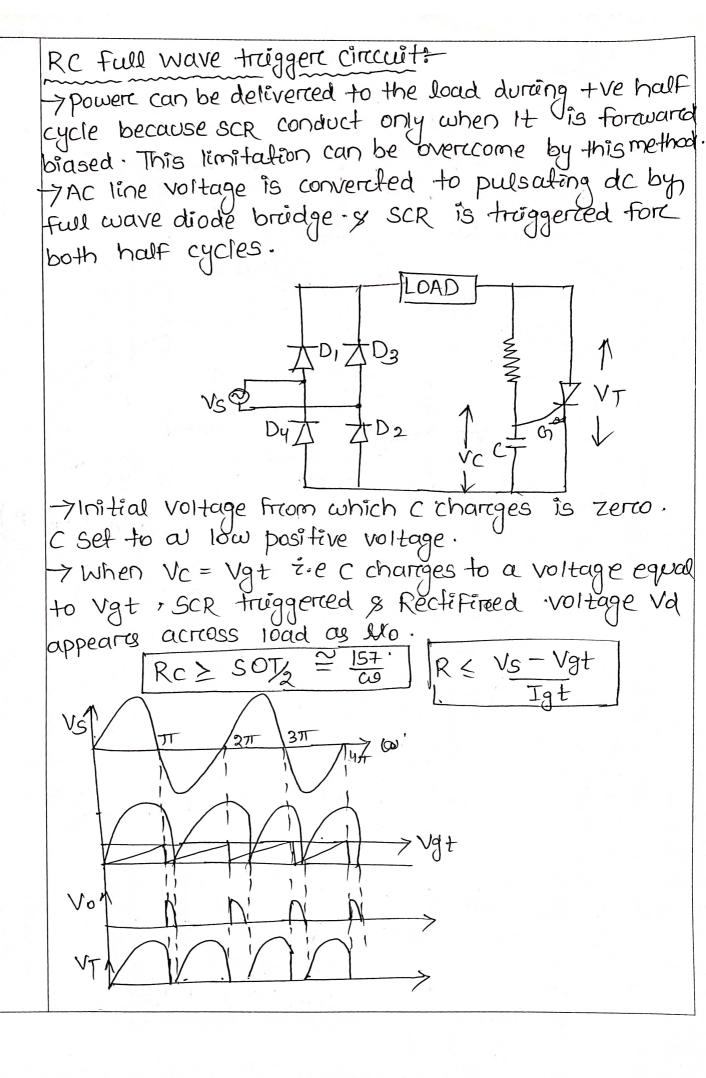


> IF Rz is large, current i is Small, as to rcesult v.d across R, t.e vg = i.R is also Vgp L Vgt Small . SCR will n't turn ON & Vo = 0, io = 0 & Supply voltage apperants across VT. 7 As firting circuit is resistive you & Vs arce in phase. K Vm sin aut \d\ 31 vgt Vgp L Vgt $\rightarrow \omega t$ Vo . lo VT →wt 71f Rz is so adjusted that | Vgp = Vgt then $Q = 90^{\circ}$

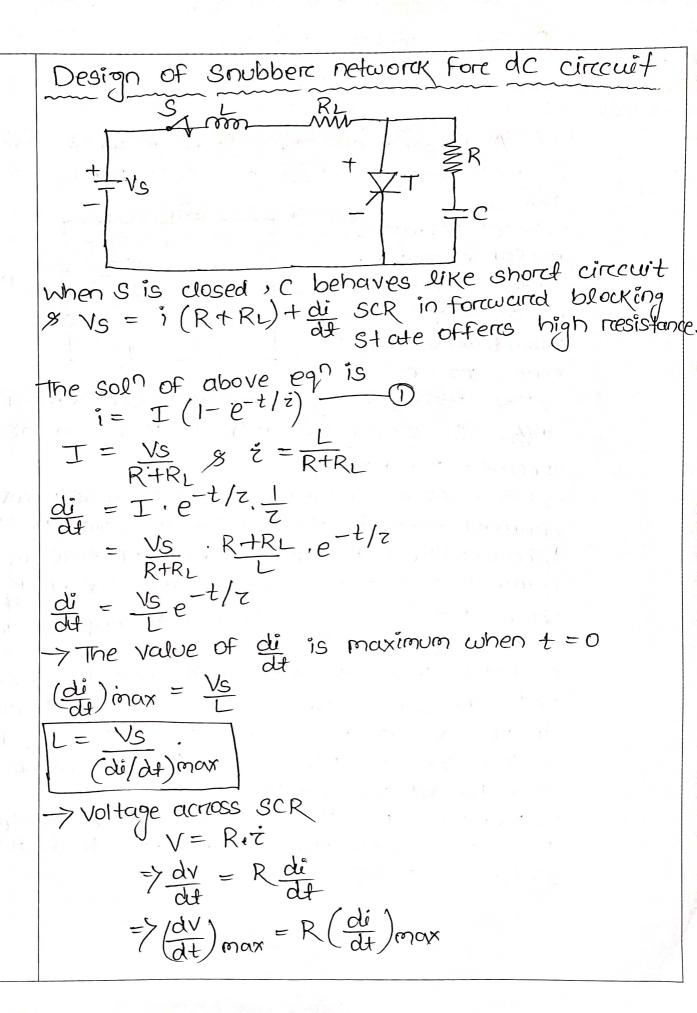
Lesson Pla	
Objectives of the Lecture	R-C Firting circuit.
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	Marker Pen. Duster. White board. Projector The limited reange of firting angle control by resistance firting ckt can be overcome by RC Firting ckt. RC half wave traggers ckt: RC half wave traggers ckt: LOAD LOAD TO THE MARKET PEN. DUSTER OF THE PROJECTOR
	Vs = Vm D, Sinwt
	(CKt diagream)
	By varying R firing angle can be controlled Load from 0° to 180°. In negative half cycle, D2 is forward biased and c charges to peak voltage - Vm through D2 with lower plate. the at wt = - JV2 Y vs depends idecreages from - Vm to 0 at 0° during this vc fall from - Vm to a lower value - oa. at wt = 0°.

In positive half cycle, D2 is reverse biased, and capacitors charges through R. Twhen Vc = Vgt, SCR is firred & after this capacifore holds a small +ve voltage. > Di is used to prevent the breakdown of gate cathode sun during - Ve half cycle. > In the range of power frequencies the RC for zerro output voltage is given by $Rc = 1.3T \approx 4$ T = 1/F = Perciod of AC line frequency in Sec. 7SCR will be triggerred when $V_1 = V_1 + V_2$ Va = Voltage dircop across Di Assume Vc = const · at the instant of truggering Igt = supplied by voltage source through R, Di & gate cathode CKt. Vs Z R Igt + Vc ZRIgt + Vgt + Vd R < Vs-Vgt-Vd where Vs is source voltage at which SCR turn ON > IF R 1 firting angle 1 R I firting angle I





Objectives of the Lecture	Design of snubberc circcuits.
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	A Snubbert CKt Consists of a servies combination of tresistance Rs & capacitance Cs is parallel with the SCR. Therefore voltage across capacitor build up at a slower dy'at, so, across SCR dy'at is less than the specified trating. Then voltage across capacitor build up at a slower dy'at, so, across SCR dy'at is less than the specified trating. Then voltage across capacitor build up at a slower dy'at, so, across SCR dy'at is less than the specified trating. Then voltage across capacitor build up at a slower dy'at, so, across SCR dy'at is less than the specified trating. Then voltage across capacitor build up at a slower dy'at, so, across scr dy'at is less than the specified trating. Then voltage across capacitor build up at a slower dy'at is less than the specified trating. The voltage across capacitor build up at a slower dy'at is less than the specified trating. The voltage across capacitor build up at a slower dy'at is less than the screen trecovery current raises to peak value at which the device blocks without Rc snubbers, the reverse recovery current cause a transient over voltage, L di in series inductance L which may destroy the device. The Rc snubbers is connected reverse recovery currents transfer to Rc path when the device blocks to full voltage Vs. When SCR is On, Cs discharges to full voltage Vs. When SCR is On, Cs discharges & Send current equal to Vs/(Resistance of local Path formed by Cs & SCR). Normally Rs, Cs L & load CKt parameters form an underestandamped ckt. So, that dy'at limited to acceptable value.



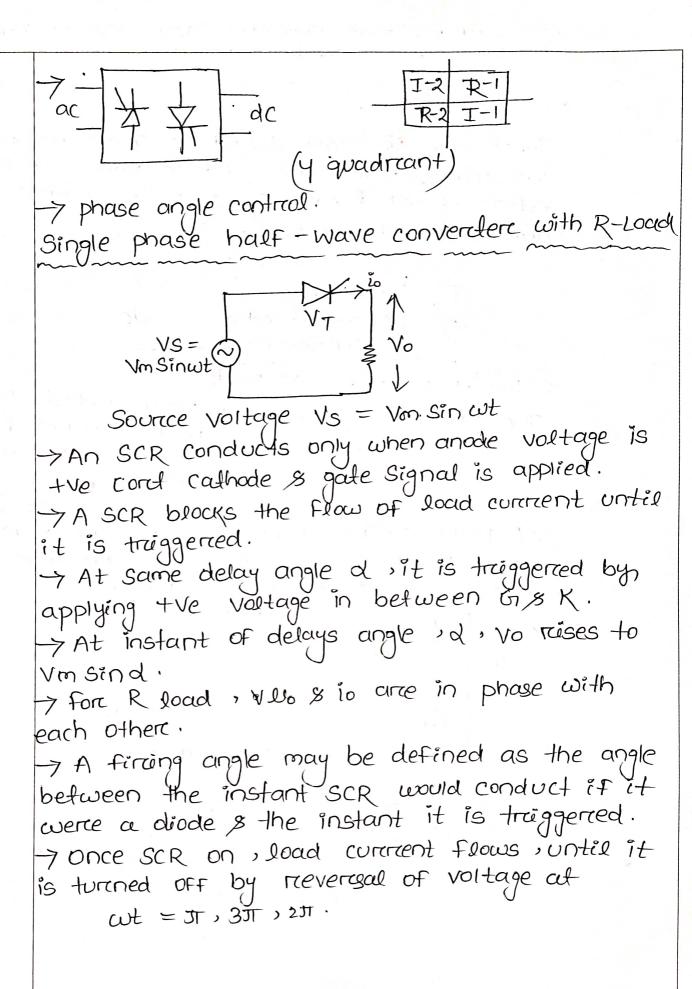
$$\Rightarrow R = \left(\frac{dv}{dt}\right) \max \frac{v_s/L}{R} = \frac{L}{v_s} \left(\frac{dv}{dt}\right) \max \left(\frac{dv}{dt}\right)$$

The parameters L, R, R, C should be \$0 Selected that the circuit becomes crutically damped. (capacitors charges in minimum time force this condition).

 $\therefore \boxed{R_L + R} = 2\sqrt{\frac{L}{C}}$ (B)

We can detercine the snubberc components R & C from eqn (A) & (B)

Objectives of the Lecture	Controlled rectifiers Techniques (phase angle, Extinction angle control, Single quadrant Semi converder.
Learning Outcomes	wight control solving quantum in servin converse cit
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	These arre line commutated at to de powers converters which arre used to convert fixed voltage, fixed frequency at powers supply into variable de olp voltage.
	Linearc Commutated dc Converter.
	The rectifier cits are Tuncontrolled (only dioder the rectifier cits are Tuncontrolled (scr)
	That controlled scr & Diode The phase controlled Rectifier may provide either a one quadrant, two quadrant or four quadrant
	-nt operation at its de tereminals.
	Tac Fac Edc Fedc > Id (one garquadrant)
	7 ac de R 2nd Quadrant)



→ single phase half wave ckt produces one pulse of load current during one cycle of vs.

→ scr conducts wt = d to IT, - -
→ over firing angle d, llo:=0

vonduction angle IT-d Uo=Us.

Objectives of the Lecture	Wordking of Single phase half wave controlled converder with Resistive load.
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	Vin Sinut Vin Sinut Vin Sinut R Vo No Scr conducts only when anode voltage is the sequence of sequ

Varyo =
$$\frac{1}{2\pi}\int^{\pi}Vm \sin \omega t d(\omega t)$$

= $\frac{Vm}{2\pi}\left(-\cos \omega t\right)^{\pi} = \frac{Vm}{2\pi}\left(1+\cos d\right)$

Maxim any value vo occurs at $d=0$
 $Vom = \frac{Vm}{2\pi} \cdot 2 = Vm/3\pi$

To = $\frac{Vo}{R} = \frac{Vm}{2\pi}\left(1+\cos d\right)$

Vorc = $\frac{1}{2\pi}\int^{\pi}Vm^{2}\sin^{2}\alpha t d\omega t$
 $= \frac{Vm^{2}}{4\pi}\int^{\pi}(\pi-d)-\frac{(\sin 2\omega t)^{\pi}}{2}$

= $\frac{Vm^{2}}{4\pi}\int^{\pi}(\pi-d)+\frac{1}{2}(\sin 2\theta)$

Vorc = $\frac{Vm}{2\sqrt{\pi}}\int^{\pi}(\pi-d)+\frac{1}{2}\sin 2\theta$

I orc = $\frac{Vorc}{R}$

P = Vorc · Torc = Power delivared to R load i/p VA = (Vs) rems Torc z/p VA

 $= \frac{Vm}{2\pi}\int^{\pi}(\pi-d)+\frac{1}{2}\sin 2\theta$
 $= \frac{Vm}{2\pi}\int^{\pi}(\pi-d)+\frac{1}{2}\sin 2\theta$
 $= \frac{Vm}{2\pi}\int^{\pi}(\pi-d)+\frac{1}{2}\sin 2\theta$
 $= \frac{Vm}{2\pi}\int^{\pi}(\pi-d)+\frac{1}{2}\sin 2\theta$

Objectives of the Lecture	Working of single-phase half wave contralled converters with
Learning Outcomes	R-L Load load & underest and need of free wheeling diade.
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	TO NO
T. F. Try	10///
	-7 At wt = d, SCR is
	träggerced.
	-> But, the inductance I torcces the load / D/P (Circle) 12
	to reise greadually 8 pnergy is stored in inductor. 7 After 8 sometime in reaches maxim value 8 then
	> After & sometime to reaches maxing value & then
	begins to decrease. -> -Ve ha cycle scurcrent continues till the energy storced in L is dissipated in R & a parch of
	energy is fed back to source. The cut = JT, Vs = 0, Vo = 0, but \$\bar{z}_0 \neq 0\$ because
	of the load inductance L.
	of the load madetained - 7 After wt = JT, SCR is subsected to rreverge anode voltage but not turned off os io not
	anode voltage ou
	less than IH. THE Some angle BTT, io = 0 & SCR turned off The biased.
	as it is already reverge biased.

7 During Free wheeling diperiod, load current doesn't delay to zero untill SCR is triggered again at 21 Fd. 0 Vo 1311 27 ίο T01 ITO KFD-> iT BIT id

A vertage load voltage,
$$V_0 = \frac{R}{\omega L}(B-\alpha)^2$$

A vertage load voltage, $V_0 = \frac{L}{\omega L}$ V_0 V_0

At $\omega t = B$, $\hat{i}_n = 0$

Objectives of the Lecture	Working of Single phase befully controlled converters with resistive load.
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
	Single phase Full Wave converderc:
Actual lecture in details with fig.	(Mid point Converter (M-2) 7 Also Called two pulse converter. 7 Single phase transformer with Centre tapped + Secondary winding, 2 SCR employed. 7 Terraninal a is the w.r.t m, n is the w.r.t b, van = Vnb Van = -Vbn
	Resistive load: 7 During the half cycle, terrminal a is the wire to ive half cycle, terrminal a is the wire to ive half cycle, terrminal a is the two wirest biased wirest biesed and delay angle d.
A TATE	Van = Vm Sinwt Vbn = -Vm Sinwt Vab = Van + Vnb = 2 Vm Sinwt At wt = d, T, is triggered Reverse Voltage across T2Van VT - Vbn + Van - VT, = 0 - Vbn Ta
	$VT_{2} = V_{bn} - V_{an} + V_{T_{1}}$ $= V_{bn} - V_{an}$ $= -V_{n} \sin d - V_{m} \sin d$ $= -2V_{m} \sin \omega t$ $= -2V_{m} \sin \omega t$

>Ti conducts from 0 to JT. -> At wt = or, Ti is reverse biased, Tais traggered at JT+d. Reverge voitage across T, = 2 Vm sin act Vs1 0 $> \omega_t$ rmsind ys Twt व्या व्याप्त 2Vm 2 Vm \gtrsim_t

Objectives of the Lecture	Working of single phase fully controlled converder with
Learning Outcomes	
Tools Used	Marker Pen, Duster, White board, Projector
Actual lecture in details with fig.	Van P (equivalent ckt) P Supply is provided through a transformer whose Secondary is centre tapped. Turn reation of primary to each secondary 1: 1. To is the centre and a, b are two terminals. The centre two terminals. The centre two terminals. The centre tapped. The centre tap

=> VT2 = Vbn - Van + VT, (VT, = 0 ag Ti is conducting)
=> VT2 = -Vm sind - Vm Sind
=-2 Vm sind.

The state of the s

TAFter wt = JT, T, is reverge biased but it'll continue conducting as the foreward biased

SCR To is not traggerred.

The strangerred of magnitude of the sind and biased by voltage of magnitude of the total current is transferenced from Toto To To

