ACADEMIC LESSION PLAN FOR WINTER - 2023

Dept. of Electronics & Telecommunication, Govt. Polytechnic , Balasore

Name of the Faculty: Yogasakti Yogamaya (Lecturer, E&TC)

Subject: VLSI & Embedded System

Theory : 4 P/W
Total Period s : 60 P/ Sem
Examination : 3 Hours
Sem : 5 E&TC

Internal Assessment : 20 Marks
End Semester Exam : 80marks
TOTAL MARKS : 100 Marks
Start of Class : 1.08.2023

WEEK	PERIOD	TOPIC	
1st	1st	**Unit-1: Introduction to VLSI & MOS Transistor(12)** 1.1 Historical perspective- Introduction	
	2nd	1.2 Classification of CMOS digital circuit types	
	3rd	1.3 Introduction to MOS Transistor& Basic operation of MOSFET.	
	4th	1.4 Structure and operation of MOSFET (n-MOS enhancement type) & COMS	12
2nd	1st	1.5 MOSFET V-I characteristics,	
	2nd	1.6 Working of MOSFET capacitances.	
	3rd	1.7 Modelling of MOS Transistors including Basic concept the SPICE level-1 models, the level-2 and level-3 model.	
	4th	1.8 Flow Circuit design procedures	
3rd	1st	1.9 VLSI Design Flow & Y chart	
	2nd	1.10 Design Hierarchy	
	3rd	1.11 VLSI design styles-FPGA, Gate Array Design,	
	4th	Standard cells based, Full custom	
4th	1st	**Unit-2: Fabrication of MOSFET (10)** 2.1 Simplified process sequence for fabrication	
	2nd	2.2 Basic steps in Fabrication processes Flow	
	3rd	2.3 Fabrication process of nMOS Transistor	
	4th	2.4 CMOS n-well Fabrication Process Flow	10
5th	1st	2.5 MOS Fabrication process by n-well on p-substrate	
	2nd	2.6 CMOS Fabrication process by P-well on n-substrate	
	3rd	2.7 Layout Design rules	
	4th	2.8 Stick Diagrams of CMOS inverter	
6th	1st	**Unit-3:MOS Inverter(09)** 3.1 Basic nMOS inverters,	
	2nd	3.2 Working of Resistive-load Inverter	
	3rd	3.3 Inverter with n-Type MOSFET Load – Enhancement Load,	
	4th	Depletion n-MOS inverter	
7th	1st	3.4 CMOS inverter – circuit operation and :	9
	2nd	characteristics and interconnect effects Delay time definitions	
	3rd	3.5 CMOS Inventor design with delay constraints Two sample mask lay out for p-type substrate.	

	4th	**Unit-4: Static Combinational, Sequential, Dynamics logic circuits & Memories(15)** 4.1 Define Static Combinational logic ,working of Static CMOS logic circuits (Two-input NAND Gate)
8th	1st	4.2 CMOS logic circuits (NAND2 Gate)
	2nd	4.3 CMOS Transmission Gates(Pass gate)
	3rd	4.4 Complex Logic Circuits - Basics
	4th	4.5 Classification of Logic circuits based on their temporal behaviour
9th	1st	**Continue**
	2nd	4.6 SR Flip latch Circuit,
	3rd	**Continue**
	4th	4.7 Clocked SR latch only.
10th	1st	**Continue**
	2nd	4.8 CMOS D latch.
	3rd	4.9 Basic principles of Dynamic Pass Transistor Circuits
	4th	4.10 Dynamic RAM,
11th	1st	SRAM,
	2nd	4.11 Flash memory
	3rd	**Unit-5: System Design method & synthesis (04)** 5.1 Design Language (SPL & HDL)& HDL & EDA tools
	4th	VHDL and packages Xlinx
12th	1st	5.2 Design strategies
	2nd	concept of FPGA with standard cell based design
	3rd	VHDL for design synthesis using CPLD or FPGA
	4th	5.3 VHDL for design synthesis using CPLD or FPGA
13th	1st	5.4 Raspberry Pi - Basic idea
	2nd	5.4 Raspberry Pi - Basic idea
	3rd	**Unit-6: Introduction to Embedded Systems(10)** 6.1 Embedded Systems Over view ,list of embedded systems, characteristics ,
	4th	example – A Digital Camera
14th	1st	6.2 Embedded Systems Technologies--Technology – Definition. -Technology for Embedded Systems
	2nd	Processor Technology, IC Technology
	3rd	6.3 Design Technology-Processor Technology, General Purpose Processors – Software,
	4th	Basic Architecture of Single Purpose Processors – Hardware
15th	1st	6.4 Application – Specific Processors,Microcontrollers,Digital Signal Processors(DSP)
	2nd	6.5 IC Technology- Full Custom / VLSI,Semi-Custom ASIC
	3rd	(Gate Array & Standard Cell), PLD (Programmable Logic Device)
	4th	6.6 Basic idea of Arduino micro controller

1/8/23

4/8/23