



ACADEMIC LESSON PLAN FOR WINTER - 2023

Dept. of Electronics & Telecommunication, Govt. Polytechnic, Balasore

Name of the Faculty: Yogasakti Yogamaya (Lecturer, E&TC)

DIGITAL ELECTRONICS (TH-3)

Theory : 4 P/W
 Total Periods : 60 P/ Sem
 Examination : 3 Hours
 Sem : 3rd E&TC

Internal Assessment : 20 Marks
 End Semester Exam : 80marks
 TOTAL MARKS : 100 Marks
 Start of Class : 1.8.2023

WEEK	PERIOD	TOPIC
1st	1 st	Unit-1: Basics of Digital Electronics 1.1 Number System-Binary, Octal, Conversion from one system to another number system.
	2 nd	Decimal, Hexadecimal - Conversion from one system to another number system.
	3 rd	1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division,
	4 th	1's & 2's complement of Binary numbers & Subtraction using complements method
2 nd	1 st	1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes, excess-3 and Gray codes.
	2 nd	1.4 Logic gates: AND, OR, NOT, NAND, -Symbol, Function, expression, truth table & timing diagram
	3 rd	NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram
	4 th	1.5 Universal Gates & its Realisation
3 rd	1 st	1.6 Boolean algebra, Boolean expressions, Demorgan's Theorems.
	2 nd	1.7 Represent Logic Expression: SOP & POS forms
	3 rd	1.8 Karnaugh map (3 & 4 Variables) &
	4 th	Minimization of logical expressions, don't care conditions
4 th	1 st	Unit-2: Combinational logic circuits 2.1 Half adder, Full adder
	2 nd	Half Subtractor, Full Subtractor,
	3 rd	Serial Binary 4 bit adder.
	4 th	Parallel Binary 4 bit adder.
5 th	1 st	2.2 Multiplexer (4:1),
	2 nd	De- multiplexer (1:4)
	3 rd	Decoder,
	4 th	Encoder
6 th	1 st	Digital comparator (3 Bit)
	2 nd	Continue...
	3 rd	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit of above)
	4 th	Seven segment Decoder (truth table, Applications of above)
7 th	1 st	Unit-3: Sequential logic Circuits 3.1 Principle of flip-flops operation, its Types,
	2 nd	3.2 SR Flip Flop using NAND Latch (un clocked)
	3 rd	SR Flip Flop using NOR Latch (un clocked)

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	4 th	3.3 Clocked SR Flip Flop-Symbol, logic Circuit, truth table and applications	
8 th	1 st	D Flip Flop-Symbol, logic Circuit, truth table and applications	
	2 nd	JK FLIP FLOP-Symbol, logic Circuit, truth table and applications	
	3 rd	T Flip Flop-Symbol, logic Circuit, truth table and applications	
	4 th	JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications	12
9 th	1 st	Continue...	
	2 nd	3.4 Concept of Racing and how it can be avoided.	
	3 rd	4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM, PS RAM	
	4 th	4.6 Basic concept of PLD & applications	
10 th	1 st	Unit-4: Registers, Memories & PLD 4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out	
	2 nd	4.2 Universal shift registers-Applications.	
	3 rd	4.3 Types of Counter & applications	8
	4 th	Asynchronous ripple counter (UP & DOWN),	
11 th	1 st	Asynchronous ripple counter (UP & DOWN),	
	2 nd	4.4 Binary counter,	
	3 rd	Decade counter.	
	4 th	Synchronous counter,	
12 th	1 st	Ring Counter	
	2 nd	Unit-5: A/D and D/A Converters 5.1 Necessity of A/D and D/A converters.	
	3 rd	5.2 D/A conversion using weighted resistors methods.	
	4 th	5.3 D/A conversion using R-2R ladder (Weighted resistors)network.	
	5 th	5.4 A/D conversion using counter method.	
13 th	1 st	5.5 A/D conversion using Successive approximate method	
	2 nd	Continue.....	16
	3 rd		
	4 th	Unit-6: LOGIC FAMILIES	
14 th	1 st	6.1 Various logic families	
	2 nd	categories according to the IC fabrication process	
	3 rd	6.2 Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation	
	4 th	Noise Margin ,Power Supply requirement &Speed with Reference to logic families.	
15 th	1 st	6.3 Features, circuit operation &various applications of TTL(NAND)	
	2 nd	CONTINUE....	
	3 rd	Features, circuit operation &various applications of CMOS (NAND)	
	4 th	Features, circuit operation &various applications of CMOS (NOR)	

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1/8/23

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