

**GOVERNMENT POLYTECHNIC, BALASORE**

Government of Odisha

ସରକାରୀ ବହୁବୃତ୍ତି ଅନୁଷ୍ଠାନ, ବାଲେଶ୍ଵର

LESSON PLAN (WINTER-2026)**Discipline: ELECTRICAL
ENGINEERING****Semester: 5th****Name of the Teaching Faculty: DEBASISH MOHAPATRA****Subject: Digital
Electronics and
Microprocessor/Code
No: EEPC301/TH-1****No of Days /per
week class
allotted: 3****Semester From date: 14TH JULY, 2026
No of Weeks: 15****Week****Class Day****Theory / Practical Topics****1st**

1st

Unit No. I:Digital Fundamentals Number Systems – Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements,

2nd

Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes

3rd

Boolean theorems, Logic gates and truth tables

2nd

1st

Universal gates

2nd

Sum of products Minterms .

3rd

Product of sum Maxterms,.

3rd

1st

Karnaugh map Minimization

2nd

Quine Mc Cluskey method of minimization

3rd

Unit No II: Combinational & Synchronous Sequential Circuits Design of Half**4th**

1st

Sequential Circuits Design of Half and Full Adders,

2nd

Sequential Circuits Design of Half and Full Subtractors,

3rd

Binary Parallel Adder -Multiplexer, Demultiplexer

5th

1st

Decoders, and Priority Encoder

2nd

Flip flops – SR, JK, T, D, design of clocked sequential circuits

3rd

Flip flops – SR, JK, T, D, design of clocked sequential circuits

6th

1st

Design of Counters- Shift registers, Universal Shift Register

2nd

Design of Counters- Shift registers, Universal Shift Register.

3rd

Unit No. III Asynchronous Sequential Circuits**7th**

1st

And Memory Devices

2nd

Stable and Unstable states, output specifications, cycles and races,

3rd

State reduction, race free assignments, Hazards,.

8th

1st

Essential Hazards, Pulse mode sequential circuits, Design of Hazard free circuits

2nd

Basic memory structure – ROM -PROM – EPROM – EEPROM EAPROM, RAM – Static and dynamic RAM–

3rd

Basic memory structure – ROM -PROM – EPROM – EEPROM EAPROM, RAM – Static and dynamic RAM–

9th

1st

Programmable Logic Devices – Programmable Logic Array (PLA) – Programmable Array Logic (PAL)

2nd

Field Programmable Gate Arrays (FPGA).

3rd

Unit No. IV: 8085 Processor Hardware Architecture,**10th**

1st

8085 Processor Hardware Architecture

2nd

pin diagram

	3rd	Functional Building Blocks of Processor
11th	1st	Memory organization – I/O ports and data transfer concepts–.
	2nd	Memory organization – I/O ports and data transfer concepts–.
	3rd	Timing Diagram Interrupts
12th	1st	Timing Diagram Interrupts
	2nd	Timing Diagram – Interrupts
	3rd	Unit No. V: Programming Processor Instruction
13th	1st	format and addressing modes
	2nd	Assembly language format
	3rd	Assembly language format
14th	1st	Data transfer
	2nd	data manipulation & control instructions
	3rd	Programming: Loop structure with counting & Indexing
15th	1st	Look up table
	2nd	Subroutine instructions
	3rd	Stack -8255 architecture and operating modes.

Debarish Mohapatra

Faculty

[Signature]
14/07/26
HOD